1996, now U.S. patent 5,991,517; which is a continuation of U.S. patent application 08/174,768, filed December 29, 1993, now U.S. patent 5,602,987; which is a continuation of U.S. patent application 07/963,838, filed October 20, 1992, now U.S. patent 5,297,148; which is a division of U.S. patent application 07/337,566, filed April 13, 1989, now abandoned. U.S. patent 5,774,395 issued from application number 757,987 filed November 27, 1996. This patent does not claim priority to another patent. U.S. patent 5,828,601 issued from application number 160,582 filed December 1, 1993. This patent also does not claim priority to another patent.

Therefore, applicants believe that applicants are the senior party in any interference proceedings.

Under M.P.E.P. § 2307 and 37 C.F.R. § 1.607, applicants request this interference be declared between the present application and the unexpired U.S. patents 5,744,395 and 5,828,601, and have satisfied each requirement of 37 C.F.R. § 1.607 as follows:

(1) The unexpired patents are:

(a) U.S. patent 5,744,395, which issued to Richart et al. on June 30, 1998; and

(b) U.S. patent 5,828,601, which issued to Hollmer et al. on October 27, 1998.

(2) The proposed counts are as follows:

Count 1

A method of operating a nonvolatile memory comprising the steps of:

programming a plurality of threshold voltages in a reference storage, the threshold voltages defining a plurality of data states of an individual memory cell of the nonvolatile memory;

electrically erasing selected ones of the programmed plurality of threshold voltages in the reference storage; and

fine-tune programming the selected ones of the programmed plurality of threshold voltages in the reference storage.

Count 2

A circuit comprising:

an interface circuit for interfacing to a nonvolatile memory, the nonvolatile memory including an individual memory cell, the interface circuit including a comparing circuit for comparing a data level of the individual memory cell to a reference data level;

a programmable and electrically erasable reference cell circuit generating the reference data level of a plurality of reference data levels defining a plurality of data states of the individual memory cell;

a first plurality of conductive lines coupling the interface circuit to the reference cell circuit;

a second plurality of conductive lines for coupling the interface circuit to an erase voltage source; and

a plurality of switches alternatively blocking the first plurality of conductive lines while coupling the second plurality of conductive lines and coupling the first plurality of conductive lines while blocking the second plurality of conductive lines.

Count 3

A memory circuit for operating a nonvolatile memory comprising:

a reference storage;

means coupled to the reference storage for programming a plurality of threshold voltages in the reference storage, the threshold voltages defining a plurality of data states of an individual memory cell of the nonvolatile memory;

means coupled to the reference storage for electrically erasing selected ones of the programmed plurality of threshold voltages in the reference storage; and

means coupled to the reference storage for fine-tune programming the selected ones of the programmed plurality of threshold voltages in the reference storage.

Count 4

A memory comprising:

an array cell having an output, an array threshold value set to one of n array threshold values to control a signal provided at the array cell output, and a gate;

a reference cell having an output, a floating gate which stores an electrical charge to allow a reference threshold value to be programmed, and a gate, the reference cell having its reference threshold value programmed between two successive ones of the n array threshold values to control a signal provided at the reference cell output;

a comparison circuit coupled to the array cell output and the reference cell output, the comparison circuit for comparing the signal at the array cell output to the signal at the reference cell output and providing a signal indicating which of the n array threshold values is held by the array cell; and

a power supply for supplying a supply voltage to the gate of the array cell to enable the array cell to provide the signal at the array cell output, the power supply further supplying the supply voltage to the gate of the programmable reference cell to enable the reference cell to provide the signal at the reference cell output.

Proposed count 1 corresponds to claim 9 of U.S. patent 5,744,395. Proposed count 2 corresponds to claim 1 of U.S. patent 5,744,395. Proposed count 3

corresponds to claim 16 of U.S. patent 5,744,395. Proposed count 4 corresponds to claim 1 of U.S. patent 5,828,601.

(3) It is respectfully submitted that claims 1-26 of U.S. patent 5,744,395 and claims 1-16 of U.S. patent 5,828,601 correspond to the proposed counts. Claim 9 of U.S. patent 5,744,395 corresponds exactly to proposed count 1. Claims 10-15 of U.S. patent 5,744,395 correspond substantially to proposed count 1 since they would have been obvious in view of the proposed count. Claim 1 of U.S. patent 5,744,395 corresponds exactly to proposed count 2. Claims 2-8 and 23-26 of U.S. patent 5,744,395 correspond substantially to proposed count 2 since they would have been obvious in view of the proposed count. Claim 16 of U.S. patent 5,744,395 corresponds exactly to proposed count 3. Claims 17- 22 of U.S. patent 5,744,395 correspond substantially to proposed count 3 since they would have been obvious in view of the proposed count. Claim 1 of U.S. patent 5,828,601 corresponds exactly to proposed count 4. Claims 2-16 of U.S. patent 5,828,601 correspond substantially to proposed count 4 since they would have been obvious in view of the proposed count. As is required under 37 C.F.R. § 1.606, the proposed counts are not narrower in scope than any patent claim designated to correspond to the proposed counts.

(4) It is respectfully submitted that claims 63-80 of the present application correspond to the proposed counts 1-4. Claim 63 of the present application corresponds exactly to proposed count 1. Claims 64-68 of the present application correspond substantially to proposed count 1 since they would have been obvious in view of the proposed count. Claim 75 corresponds exactly to proposed count 2. Claim 69 of the present application corresponds exactly to proposed count 3. Claims 70-74 correspond substantially to proposed count 3 since they would have been obvious in view of the proposed count. Claim 76 of the present application corresponds exactly to proposed count 4. Claims 77-80 correspond substantially to proposed count 4 since they would have been obvious in view of the proposed count. Per 37 C.F.R. § 1.606, the proposed counts 1-4 are not narrower in scope than any application claim designated to correspond to the proposed counts 1-4.

(5) Examples of support for the claims are found throughout the specification as originally filed on April 13, 1989 in parent application 07/337,566. Once again, the present application (09/310,880, filed May 14, 1999) is a continuation of U.S. patent application 08/771,708, filed December 20, 1996, now U.S. patent 5,991,517; which is a continuation of U.S. patent application 08/174,768, filed December 29, 1993, now U.S. patent 5,602,987; which is a continuation of U.S. patent application 07/963,838, filed October 20, 1992, now U.S. patent 5,297,148; which is a division of U.S. patent application 07/337,566, filed April 13, 1989, now abandoned. For convenience, issued U.S. patent application (U.S. patent 5,991,517) is being used to identify support for the claims. Specifically, support in the issued parent application for the claims is tabulated below.

Claim 63 (Claim 9 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
63. A method of operating a nonvolatile memory comprising the steps of:	The application states at column 1, lines 15-18 and 30-32 the invention relates generally to nonvolatile memories. Some specific examples of nonvolatile memories are EEPROM and Flash EEPROM devices. Some methods of operating the nonvolatile memory are described in the "Summary of the Invention" section of the application. Further, Figure 19 and the corresponding description starting at column 25, line 24 show one method of operating a nonvolatile memory.
programming a plurality of threshold voltages in a reference storage, the threshold voltages defining a plurality of data states of an individual memory cell of the nonvolatile memory;	At column 25, lines 18-20, the application describes programming reference levels into master and local reference cells. Furthermore, the memory is divided into sectors. Each sector of the memory has local reference cells. See column 25, lines 6-11, 15-17. These reference levels serve to define two or more data states of an individual nonvolatile memory cell. See column 22, lines 51-66; column 23, lines 8-11, 34-37; column 24, lines 66-67; column 25, lines 54-56.

electrically erasing selected ones of the programmed plurality of threshold voltages in the reference storage; and	Figure 19(1) to Figure 19(3) show a technique including electrically erasing reference cells. Further, the application describes erasing local reference cells in one sector at column 25, lines 24-27. In a specific implementation, the reference cells are EEPROM or Flash cells, which are electrically erased. See column 8, lines 29-41. Furthermore, the application states at column 23, lines 25-33 and column 24, lines 36-45, the reference cells may be independently set or reprogrammed, and that the reference threshold level may be set to an optimum level and fine-tuned.
fine-tune programming the selected ones of the programmed plurality of threshold voltages in the reference storage.	Figure 19(4) to Figure 19(7) show a technique of programming the reference cells. The application describes the programming technique at column 25, lines 36-49. The references are programmed to various breakpoint threshold levels. See column 25, lines 46-49.

Claim 64 (Claim 10 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
64. A method according to claim 63 further comprising the steps of: sensing a voltage from an individual memory cell of the nonvolatile memory;	Starting at column 24, line 10, the application describes circuitry and techniques for sensing a voltage state of a memory cell (1421). Figures 17B and 17C show the circuitry and timing diagrams.
sensing a plurality of programmed threshold voltages from the reference storage;	Figure 17B and the corresponding description in the application starting at column 24, line 10 also shows circuitry for sensing a number of programmed threshold voltages of reference cells (1431 to 1435). The reference cells may be the master or local reference cells. See Figures 20A and 20B and the description at column 25, lines 54-67.
comparing the sensed voltage from the individual memory cell to the sensed plurality of programmed threshold voltages from the reference storage; and	Figure 17B and the corresponding description in the application show circuitry (*i.e.*, sense amplifier) for comparing the sensed voltage of the memory cell (1421) to the programmed threshold voltages (of reference cells 1431 to 1435). These cells may be master or local reference cells. See Figures 20A and 20B and the description at column 25, lines 54-67.

determining a multiple-bit data value based on the comparison result.	As shown in Figure 17B and described at column 24, lines 20-31, the sense amplifier circuitry determines a multiple-bit data value (Bit 1 to Bit L) based on the comparison result.

Claim 65 (Claim 11 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
65. A method according to claim 63 wherein the step of programming a plurality of threshold voltages in a reference storage further comprises the steps of: programming an individual electrically-erasable reference cell to define a plurality of data states in the individual memory cell of the nonvolatile memory.	Figure 19(4) to Figure 19(7) show a method of programming at least one electrically erasable reference cell. The application describes the method at column 25, lines 6-7, 13-17, and 18-20. The reference cells may define two or more data states. See column 24, lines 32-33.

Claim 66 (Claim 12 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
66. A method according to claim 63 wherein the step of programming a plurality of threshold voltages in a reference storage further comprises the steps of: programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.	Figure 19(4) to Figure 19(7) show a method of programming two or more electrically erasable reference cells. The application describes the method at column 25, lines 6-7, 13-17, and 18-20. The reference cells may define two or more data states. See column 24, lines 32-33.

Claim 67 (Claim 13 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application-
67. A method according to claim 63 wherein the step of programming a plurality of threshold voltages in a reference storage further comprises the steps of: programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory; and	Figure 19(4) to Figure 19(7) show a method of programming two or more electrically erasable reference cells. The application describes the method at column 25, lines 6-7, 13-17, and 18-20. Furthermove, the application describes programming of master and local reference cells. See column 24, lines 32-48, and 60-67.

programming individual electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.	Figure 19(4) to Figure 19(7) show a method of programming at least one electrically erasable reference cell. The application describes the method at column 25, lines 18-20. Furthermore, the application describes programming of local reference cells in a separate step from programming the master reference cells. See column 24, lines 32-48 and 60-67.

Claim 68 (Claim 15 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
68. An electronic system including a processor, a memory and a system bus comprising: a memory circuit performing the method according to claim 63.	Figure 1A shows an electronic system including a processor (microprocessor 21), memory (RAM 25), and a system bus (23) with a memory circuit (33). The memory circuit 33 performs the method shown in Figure 19 and described in the application starting at column 25, line 24.

Claim 69 (Claim 16 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
69. A memory circuit for operating a nonvolatile memory comprising:	The application describes circuitry for operating a nonvolatile memory. Examples of such circuitry are shown in Figures 3A, 12, 13, 17A, 17B, and 20A and the corresponding description.

a reference storage;	Figure 17A shows a master storage cell (1400). Figure 17B shows some multistate reference cells (1431 to 1435). Figure 20 shows some local reference cells (1525). The application describes reference cells at column 23, lines 8-11 and column 25, lines 15-17, among other locations.
means coupled to the reference storage for programming a plurality of threshold voltages in the reference storage, the threshold voltages defining a plurality of data states of an individual memory cell of the nonvolatile memory;	Circuit 1410 in Figure 17A is an example of a means connected to the reference cell 1400 to program the cell. See also column 23, lines 22-28. The reference cell is used to define the data states of a multistate memory. See column 23, lines 8-15. The application describes other means to perform the recited function to the local reference cells at column 25, lines 6-24.
means coupled to the reference storage for electrically erasing selected ones of the programmed plurality of threshold voltages in the reference storage; and	Circuit 1410 in Figure 17A is an example of a means connected to the reference cell 1400 to erase the cell. See also column 23, lines 22-28. The reference cell is used to define the data states of a multistate memory. See column 23, lines 8-15. The application describes other means to perform the recited function to the local reference cells at column 25, lines 6-24.

means coupled to the reference storage for fine-tune programming the selected ones of the programmed plurality of threshold voltages in the reference storage.	Circuit 1410 in Figure 17A is an example of a means connected to the reference cell 1400 to program the cell. See also column 23, lines 22-28 and column 24, lines 36-45. The reference cell is used to define the data states of a multistate memory. See column 23, lines 8-15. The application describes other means to perform the recited function to the local reference cells at column 25, lines 6-24.

Claim 70 (Claim 17 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
70. A memory circuit according to claim 69 further comprising:	Figure 17B and the corresponding description show a sense amplifier circuit (1440) including circuitry for sensing a voltage state of an individual memory cell.
means for sensing a voltage from an individual memory cell of the nonvolatile memory;	
means coupled to the reference storage for sensing a plurality of programmed threshold voltages from the reference storage;	Figure 17B and the corresponding description show a sense amplifier circuit (1440) including circuitry connected to reference cells for sensing their threshold voltages.

means coupled to the reference storage and coupled to the nonvolatile memory for comparing the sensed voltage from the individual memory cell to the sensed plurality of programmed threshold voltages from the reference storage; and	Figure 17B and the corresponding description show a sense amplifier circuit (1440) including circuitry for comparing the voltage states sensed for the individual memory cell and the reference storage.
means coupled to the comparing means for determining a multiple-bit data value based on the comparison result.	Figure 17B and the corresponding description show a sense amplifier circuit (1440) including circuitry (1440) and decoder (1480) include circuitry to determine a multiple-bit data value based on the comparison.

Claim 71 (Claim 18 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
71. A memory circuit according to claim 69 wherein the means for programming a plurality of threshold voltages in a reference storage further comprises: means for programming an individual electrically-erasable reference cell to define a plurality of data states in the individual memory cell of the nonvolatile memory.	In an embodiment, the application describes the reference cell as being electrically erasable at column 23, line 10 (*i.e.*, EEPROM).

Claim 72 (Claim 19 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
72. A memory circuit according to claim 69 wherein the means for programming a plurality of threshold voltages in a reference storage further comprises: means for programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.	In an embodiment, the application describes the reference cells as being electrically erasable at column 23, line 10 (i.e., EEPROM). Furthermore, Figure 17A shows circuitry 1410 to program one or more reference cells. See also column 23, lines 25-28.

Claim 73 (Claim 20 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
73. A memory circuit according to claim 69 wherein the means for programming a plurality of threshold voltages in a reference storage further comprises: means for programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory; and	In an embodiment, the application describes the reference cell as being electrically erasable at column 23, line 10 (*i.e.*, EEPROM). The circuitry (1410) may be used to program two or more reference cells used to define multiple data states. See column 23, lines 16-28.

means for programming individual electrically-erasable reference cells of the plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.	In an embodiment, the application describes the reference cell as being electrically erasable at column 23, line 10 (*i.e.*, EEPROM). The circuitry (1410) may be used to program individual reference cells used to define multiple data states. See column 23, lines 16-28.

Claim 74 (similar to Claim 22, not identical)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
74. A memory circuit according to claim 69 wherein the nonvolatile memory is flash electrically-erasable and programmable memory.	In an embodiment, the memory includes Flash devices. See column 1, lines 66-67.

Claim 75 (Claim 1 of U.S. patent 5,774,395)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
75. A circuit comprising: an interface circuit for a programmable and electrically erasable reference cell circuit generating the reference data level of a plurality of reference data levels defining a plurality of data states of the individual memory cell;	Figure 17B and the corresponding description show an interface circuit (1440) that interfaces to a nonvolatile memory. The interface includes circuitry to compare a data level of an individual cell to a reference cell (*e.g.*, 1431). See column 23, lines 10-19.

a programmable and electrically erasable reference cell circuit generating the reference data level of a plurality of reference data levels defining a plurality of data states of the individual memory cell;	Figure 17B and the corresponding description show electrically erasable reference cells (1431 to 1435).
a first plurality of conductive lines coupling the interface circuit to the reference cell circuit;	Figure 17B and the corresponding description show conductive lines (1441 and lines not labeled in the figure) connected the reference circuit to the interface circuit.
a second plurality of conductive lines for coupling the interface circuit to an erase voltage source; and	Figure 17B does not show explicitly the erase circuitry. But Figure 17A and the corresponding description show erase circuitry that would be analogously used in Figure 17B. Figure 17A shows conductive lines coupling an erase voltage source (1411) to the interface circuit (1410).
a plurality of switches alternatively blocking the first plurality of conductive lines while coupling the second plurality of conductive lines and coupling the first plurality of conductive lines while blocking the second plurality of conductive lines.	Figure 17B and the corresponding description show a plurality of switches (1451 to 1455) and Figure 17A has logic in erase decode (1417) to alternatively block the connection of the reference cell to the comparison circuit or the erase voltage source (1411).

Claim 76 (Claim 1 of U.S. patent 5,828,601)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
76. A memory comprising: an array cell having an output, an array threshold value set to one of n array threshold values to control a signal provided at the array cell output, and a gate;	The application shows a memory (33 in Figures 1, 6, and 8) including an array cell with multiple thresholds (Figure 11 and 1073 in Figure 12). See column 19, lines 1-20; column 21, lines 48-51).
a reference cell having an output, a floating gate which stores an electrical charge to allow a reference threshold value to be programmed, and a gate, the reference cell having its reference threshold value programmed between two successive ones of the n array threshold values to control a signal provided at the reference cell output;	The application shows a reference cell (1400 in Figure 17A, 1431 to 1435 in Figure 17B). This reference cell may be an EEPROM cell, which is a floating gate device. See column 23, line 7. This cell is programmed with a threshold value between two successive ones of the n array threshold values. Referring to Figure 15B, I_{REF} ("2") shows a conduction curve (a signal output) for a reference cell that is between the programmed values I_{DS} ("2") and I_{DS} ("3"). See column 22, lines 58-66 and column 23, lines 5-11.

a comparison circuit coupled to the array cell output and the reference cell output, the comparison circuit for comparing the signal at the array cell output to the signal at the reference cell output and providing a signal indicating which of the n array threshold values is held by the array cell; and	Figures 17A and 17B and the corresponding descriptions show two comparison circuits (1410 in Figure 17A and 1440 in Figure 17B) to compare a reference cell output to an array memory cell output (*e.g.*, see nodes A and B in Figure 17B). The circuit provides as output SA1 through SAK which is decoded into B1 through BL, which is an indication of which threshold is held by the array memory cell.
a power supply for supplying a supply voltage to the gate of the array cell to enable the array cell to provide the signal at the array cell output, the power supply further supplying the supply voltage to the gate of the programmable reference cell to enable the reference cell to provide the signal at the reference cell output.	Figure 15B and the corresponding description show the voltage applied at V_{CG} (gate) of the reference cell (see V_{CG} of cell 1400 of Figure 17A) (indicated by I_{REF} conduction lines) and of the array cell (indicated by the I_{DS} conduction lines). As indicated by the dashed line, both V_{CG} of the array cell and reference cell are connected during reading to a power supply of 5 volts. See column 22, lines 53-66. Also see column 30, lines 2-5 and the Tables 1 and 2 in Figures 26 and 27, respectively. These describe the V_{CG} of an array cell being connected to V_{CC} during a read operation.

Claim 77 (Claim 2 of U.S. patent 5,828,601)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
77. The memory of claim 76 wherein when a value of the supply voltage is varied, a working margin between the array cell output and the reference cell output remains constant.	Figure 15B and the corresponding description show outputs of an array cell and a reference cell. As the supply voltage at V_{CG} is varied, a working margin between the outputs remains relatively constant. For example, see the conduction curves for I_{REF} ("0") and I_{DS} ("0") for V_{CG} at and near 5 volts, the I_{DS} is relatively constant. Furthermore, as V_{CG} varies, the reference levels remain between the programmed levels. Furthermore, at column 24, lines 38-42, the application describes the memory cells and reference cells tracking with similar variations in operating conditions.

Claim 78 (Claim 3 of U.S. patent 5,828,601)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
78. The memory of claim 76 wherein n is greater than two.	Figure 15B and the corresponding description show an array cell having more than 2 threshold values. In fact, four threshold values corresponding to 0, 1, 2, and 3 states are shown.

Claim 79 (Claim 14 of U.S. patent 5,828,601)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
79. A memory comprising: a first word line;	As described at column 20, lines 22-24, Figure 12 shows an array of a memory. The array has nonvolatile memory cells (1073) where control gates (V_{CG}) of a row of cells are connected to a word line (1079).
a second word line;	Figure 17A shows a reference cell (1400) with a word line (V_{CG}) connected to a gate of the reference cell.
a power supply for providing a substantially identical supply voltage to the first word line and the second word line;	Figure 15 shows the V_{CG} lines for both the array cell and reference cell are connected to the same supply voltage (*e.g.*, 5 volts) during a read operation.
an array cell having a gate connected to the first word line and a source-to-drain path, the array cell having a threshold value set to one of n array threshold values;	Figure 12 shows the array cell (1073). Figure 11 shows greater detail of an example of one type of array cell having a source-to-drain path and control gate. This array cell is a nonvolatile memory cell having n threshold values. See column 19, lines 27-33.

n-1 read reference cells, each read reference cell having a gate connected to the second word line, a source-to-drain path and a floating gate which stores an electrical charge to allow a reference threshold value to be programmed, each respective read reference cell having its reference threshold value programmed between two different successive ones of the n array threshold values; and	The application describes that for an array cell having n threshold values, there will be at least n-1 reference levels. See column 24, lines 1-2. Therefore, there will be at least n-1 read reference cells to provide these reference levels. Each reference cell is an EEPROM cell, which has a floating gate. See column 23, lines 5-8. Figure 15B shows the reference threshold values (I_{REF}) which are between two different array programmed values (I_{DS}).
read sense amplifiers, each read sense amplifier having a first input coupled to the source-to-drain path of the array cell and a second input coupled to the source-to-drain path of a respective one of the read reference cells, each read sense amplifier for providing an output signal indicating whether a signal received at its first input is greater than a signal received at its second input.	Figure 17B shows a read sense amplifier which is connected at A and B to source-to-drain paths of a reference cell and an array cell. The sense amplifier includes circuitry to compare the A and B inputs. See column 24, lines 24-27.

Claim 80 (Claim 16 of U.S. patent 5,828,601)	Support in U.S. Patent 5,991,517 (Issued Parent Application)
80. The memory of claim 79 wherein n is greater than two.	Figure 15B shows an array cell having more than two threshold values. In fact, four threshold values corresponding to 0, 1, 2, and 3 states are shown.

(6) The requirements of 35 U.S.C. § 135(b) are met because claims 63-75 were present in this application within one year of the issue date of U.S. patent 5,774,395, and claims 76-80 were present in this application within one year of the issue date of U.S. patent 5,828,601.

In particular, U.S. patent 5,774,395 issued June 30, 1998, and claims 63-75 were added into the present application on May 13, 1999. U.S. patent 5,828,601 issued October 27, 1999, and claims 76-80 were added into the present application on September 29, 1999.

CONCLUSION

In view of the foregoing, applicants believes that no new matter has been introduced. Applicants respectfully request that the examiner declare an interference under 37 C.F.R. § 1.607 between the present application and U.S. patents 5,744,395 and 5,828,601.

If the examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

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